UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,226	02/06/2004	Erik K. Norden	20658/0203688-US0	8114

38881 7590 12/15/2006

DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,226	NORDEN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1,3-8,12-16,20-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Douglas (patent No. 6,609,193).

3. Douglas taught the invention as claimed including a data processing ("DP") system comprising (as per claim 1):

a) a multithreaded processor supporting plurality of active thread (e.g., see col. 2, line 59-col. 3, line 17);

b) Instruction fetch and issue unit comprising instruction fetch stage (313) configured to fetch a plurality of sets of fetched bits (e.g., see col. 4, lines 35-41), wherein each set of fetched bits can represent a plurality of instructions (e.g., see col.6, line 50-67)[each VLIW instruction is decoded and marked off into plural instructions and therefore can represent plural instructions, the scope of the claims comprises a sequential fetching of plural sets of bits, which a VLIW instruction would meet but also since the Douglas VLIW instruction comprised at least four instructions when fetched then the grouping of two of the instructions as one plurality of fetch bits and the other two instructions as another group of bits also meets the limitation if the fetching was of the groups of bits was simultaneous (which is not specified in the claim) (e.g. see col.

7,lines 17-62) where the instructions were fetched as eight bytes regardless of the length so when single byte instructions were fetched at least four instructions would be fetched at a time]; and a pipeline coupled to the instruction fetch stage (e.g., see fig. 3) and configured to receive a set of fetched bits and an associated thread ID (e.g., see col. 4, line 42-col.5, line 53 and fig. 4).

4. As to claim 3, Douglas taught predecode stage configured to predecode each set of fetched bits (e.g., see fig. 5)(first length decoder).

5. As per claim 4,14, 22 Douglas taught the pipeline comprises a plurality of pipeline stages wherein each pipeline stage stores a thread ID (e.g., see fig. 4)(e.g., see col. 5 lines 1-53).

6. As per claim 5,15,23, Douglas taught the pipeline comprises a data forwarding unit for forwarding data from a first pipeline stage having a first thread ID to an second stage having a second thread ID (e.g., see col. 17, lines 7-50).

7. As per claim 6,16,24, Douglas taught the data forwarding unit comprises a comparator (e.g., see fig. 6 and col. 9, lines 14-36 and col. 11, lines 10-55),

8. As per claims 7,8, Douglas taught the data forwarding unit forward data when the first thread ID is equal to a second ID and prevents data forwarding when the first thread ID is not equal to the second ID (e.g., see fig. 6 and col. 12, lines 32-64 and col. 11, lines 10-55).

9. As per claims 12,20 Douglas taught means and step for fetching a first set of bits representing one or more instructions (e.g., see col. 4, lines 35-41); means and set for attaching an associate thread ID to the set of fetched bits (e.g., see col. 5, lines 1-

55)[thread-id and instruction flow in corresponding stages of two pipelines attached or linked by conductors in figure 4]; means and step for issuing the instructions of the first set of fetched bits with the associated thread ID to the pipeline)[thread-id and instruction are input or issued and flow in corresponding stages of two pipelines attached or linked by conductors in figure 4].

10. As per claims 13,21 Douglas taught means and step for reading a first operand for the first set of instructions and means and step for propagating the associated thread ID through the pipeline with the first set of instructions and operand (e.g., see fig. 4 and col. 4, lines 42-65)[the instructions/operands are decoded into UOPs that are propagated down pipeline with associated thread ID].

Claim Rejections - 35 USC § 103

11. Claims 2, and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Douglas (patent No 6,609,193).

12. Douglas taught the invention as claimed including a data processing ("DP") system comprising (as per claim 1):

a) a multithreaded processor supporting plurality of active thread (e.g., see col. 2, line 59-col. 3, line 17);

b) Instruction fetch and issue unit comprising instruction fetch stage (313) configured to fetch a plurality of sets of fetched bits (e.g., see col. 4, lines 35-41 wherein each set of fetched bits can represent a plurality of instructions (e.g., see col.6, line 50-67)[each VLIW instruction is decoded and marked off into plural instructions and therefore can represent plural instructions, the scope of the claims comprises a

sequential fetching of plural sets of bits, which a VLIW instruction would meet but also since the Douglas VLIW instruction comprised at least four instructions when fetched then the grouping of two of the instructions as one plurality of fetch bits and the other two instructions as another group of bits also meets the limitation if the fetching was of the groups of bits was simultaneous (which is not specified in the claim) (e.g. see col. 7,lines 17-62) where the instructions were fetched as eight bytes regardless of the length so when single byte instructions were fetched at least four instructions would be fetched at a time]; and a pipeline coupled to the instruction fetch and issue unit (e.g., see fig. 3) and configured to receive a set of fetched bits and an associated thread ID (e.g., see col. 4, line 42-col.5, line 53 and fig. 4).); and a pipeline coupled to the instruction fetch stage (e.g., see fig. 3) and configured to receive a set of fetched bits and an associated thread ID (e.g., see col. 4, line 42-col.5, line 53 and fig. 4).

13. As per claims 12,20 Douglas taught means and step for fetching a first set of bits representing one or more instructions (e.g., see col. 4, lines 35-41); means and set for attaching an associate thread ID to the set of fetched bits (e.g., see col. 5, lines 1-55)[thread-id and instruction flow in corresponding stages of two pipelines attached or linked by conductors in figure 4]; means and step for issuing the instructions of the first set of fetched bits with the associated thread ID to the pipeline)[thread-id and instruction are input or issued and flow in corresponding stages of two pipelines attached or linked by conductors in figure 4].

14. As per claim 2, Douglas taught the fetch and issue unit comprises an instruction buffer coupled to the instruction fetch stage and configured to store the sets of fetched bits and (e.g., see col. 6, lines 17-62) [thread specific buffer 502A store instructions of a thread] Douglas however did not expressly detail the buffer storing the associated thread ID for each set of fetched bits. Douglas however taught the buffer 502A duplicates thread ID as instructions are output until the buffer 502A is cleared. Therefore One of ordinary skill would have been motivated to store the thread ID in the buffer at least because the buffer is thread ID specific storing the instruction of the specific thread and duplicating the thread ID and sending the thread ID with each output instruction. Storing the thread ID in the buffer would have simplified the operation of retrieval of the thread ID for duplicating the thread ID.

15. As per claims 28,29,30,31,32 Douglas taught coupling an element (315) that indicated that a next trace instruction that was output to a trace cache which as coupled to the instruction decoder 316 and a memory controller (313) for controlling the storing of traces and access to traces when a trace could be used by a process (e.g., see col. 4, lines 22-41). Douglas taught each VLIW instruction (and each of the decoded instructions from the VLIW instruction have an associated instruction ID (e.g., see fig. 4) Therefore one of ordinary skill would have been motivated to couple a trace unit that monitors fetched bits and associated thread ID to the fetch and issue unit. Further, since the instructions were variable length the one of ordinary skill would have been motivated to compress the trace stored in the trace cache at least conserve space in the cache for

instruction that did not require the maximum number of bits (e.g., see col. 7, lines 17-62).

16. Claims 9-11,17-19,25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Douglas as applied to claims 1,12,20 above, and further in view of Joy (patent No. 6,507,862).

17. As per claims 9-11, 17-19, 25-27 Joy taught a very fast exception handling logic includes connection of and exception signal or trap to evoke a switch in thread state and machine state where the switch in thread state or machine state causes the processor to enter and exit the exception handler immediately without invoking the operating system. (e.g., see col. 15, lines 8-26). Joy also taught thread reservations in which a thread pathway is reserved for usage by a selected thread (e.g., see col. 16, lines 9-60). Therefore it would have been obvious to one of ordinary skill that the exception or trap handler that controlled thread switching on a priority basis would have resolved the trap when the highest priority thread was present an stalled the trap when a lesser priority thread was present.

18. It would have been obvious to one of ordinary skill to combine the teachings of Douglas and Joy. Both references were directed toward the problems for execution multiple thread in a data processing system. Since both references processed plurality of threads on a pipeline one of ordinary skill would have motivated to incorporate the exception handling logic of Joy at least to facilitate the switching between the threads in the combined system especially when there was at stall in a thread in the pipeline due

to memory access (e.g. see col. 7, lines 54-62 of Douglas and col. 8, lines 46-60 of Joy).

Response to Arguments

19. The change in scope of the amended claims has necessitated a new search.

20. Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER